What Is Claimed Is:

1. A bus bridge circuit, which issues a read request to a first device in response to a read request from a second device, receives data from said first device via a first bus, and transfers the data to said second device via a second bus, comprising:

a data buffer, which receives and stores the data of said first device, and error detection information generated from said data and from byte enable signals specifying, in units of a prescribed number of bits, the parallel data from said bus bridge circuit on said first bus to be enabled;

an error detection information generation circuit, which generates new error detection information from byte enable signals specifying, in units of a prescribed number of bits, the parallel data from said second device on said second bus to be enabled, and from error detection data received in said data buffer; and

a controller, which transfers to said second device via said second bus the data of said data buffer and said new error detection information, in response to said byte enable signals of said second device.

2. The bus bridge circuit according to Claim 1, wherein said controller transmits to said first device said byte enable signal in order to pre-fetch the data of said first device.

3. The bus bridge circuit according to Claim 1, wherein said error detection information generation circuit comprises an XOR circuit which takes the XOR of said byte enable signal from said second device and a parity bit received in said data buffer.

4. The bus bridge circuit according to Claim 1, wherein said controller transmits said byte enable signals in sequence to said first device, in response to ready signals from said first device responding to said read request sent to said first device, transmits a ready signal to said second device after storing data from said first device in said data buffer, and receives byte enable signals from said second device.

5. The bus bridge circuit according to Claim 1, wherein said data buffer comprises a FIFO buffer.

6. A bus connection system comprising:

a second device which issues read requests;

a first device which outputs read data in response to said read requests; and

a bus bridge circuit which is connected to said second device by a second bus and is connected to said first device by a first bus, and transfers the read data from said first device via said first bus to said second device via said second bus,

wherein said first device outputs to said first bus said read data and error detection information generated from said data and a byte enable signals specifying, in units of a prescribed number of bits, the parallel data from said bus bridge circuit on said first bus to be enabled,

and wherein said bus bridge circuit has:

a data buffer which receives and stores said read data and said error detection information from said first device;

an error detection information generation circuit which generates new error detection information from a byte enable signal specifying, in units of a prescribed number of bits, the parallel data from said second device on said second bus to be enabled, and from error detection information received in said read buffer; and

a controller which transfers the data of said data buffer and said new error detection information to said second device via said second bus, in response to said byte enable signals of said second device.

7. The bus connection system according to Claim 6, wherein said controller transmits to said first device said byte enable signals in order to pre-fetch the data of said first device.

8. The bus connection system according to Claim 6, wherein said error detection information generation circuit comprises an XOR circuit which takes the XOR of the byte

enable signals from said second device and of the error detection information received in said data buffer,

and wherein said first device has an XOR circuit which generates said error detection information from said byte enable signals from said bus bridge circuit and from said read data.

9. The bus connection system according to Claim 6, wherein said controller transmits said byte enable signals in sequence to said first device in response to ready signals from said first device responding to said read request sent to said first device, and after storing data from said first device in said data buffer, transmits a ready signal to said second device, and receives a byte enable signal from said second device.

10. The bus connection system according to Claim 6, wherein said data buffer comprises a FIFO buffer.

11. A data error notification method for a bus bridge circuit for issuing a read request to a first device in response to a read request from a second device, receiving data from said first device via a first bus and transferring the data to said second device via a second bus, comprising:

a step of receiving and storing in a data buffer the data of said first bus and error detection information generated from said data and from byte enable signals

specifying, in units of a prescribed number of bits, the parallel data from said bridge circuit on said first bus to be enabled;

an error detection information generation step of generating new error detection information from byte enable signals specifying, in units of a prescribed number of bits, the parallel data from said second device on said second bus to be enabled, and from error detection information received in said data buffer; and

a step of transferring to said second device via said second bus the data of said data buffer and said new error detection information, in response to said byte enable signals of said second device.

12. The data error notification method for a bus bridge circuit according to Claim 11, further comprising a step of transmitting to said first device said byte enable signals in order to pre-fetch data of said first device.

13. The data error notification method for a bus bridge circuit according to Claim 11, wherein said error detection information generation step comprises a step of taking the XOR of the byte enable signals from said second device and of the error detection information received in said data buffer.

14. The data error notification method for a bus

bridge circuit according to Claim 11, further comprising:

a step of transmitting said byte enable signals in sequence to said first device in response to ready signals from said first device responding to said read request sent to said first device; and

a step of transmitting a ready signal to said second device after storing data from said first device in said data buffer, and receiving byte enable signals from said second device.

15. The data error notification method for a bus bridge circuit according to Claim 11, wherein said storage step comprises a step of storing said read data and error detection information in a data buffer which is a FIFO buffer.